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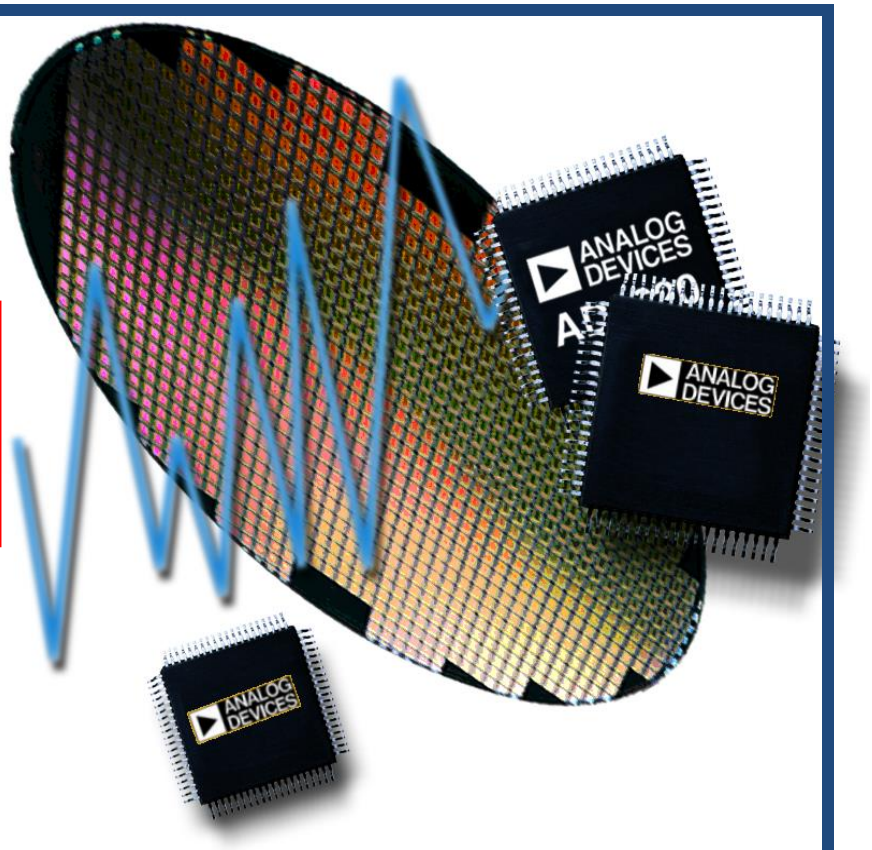

Reliability Report

Report Title: ADUCM430 Die Attach Film Qualification

Report Number: 18956

Revision: A

Date: 13 June 2022

Summary

This report documents the successful completion of the reliability qualification requirements for the release of the ADUCM430 product in a 121-CSP_BGA package with the Hitachi HR5104 Die Attach Film. The ADUCM430 is a Precision Analog Microcontroller for 400G+ Direct Detection Optical Module.

Description / Results of Tests Performed

Tables 1 and 2 provide a description of the qualification tests conducted and the associated test results for products manufactured on the same technologies as described in Table 1. All devices were electrically tested before and after each stress. Any device that did not meet all electrical data sheet limits following stressing would be considered a valid (stress-attributable) failure unless there was conclusive evidence to indicate otherwise.

Table 1: CSP_BGA at STATS (SC3) Package Qualification Test Results

Test Name	Specification	Conditions	Device	Lot #	Sample Size	Qty. Failures
High Temperature Storage Life (HTSL)	JESD22-A103	150°C, 1,000 Hours	ADUCM430	Q18956.1.HS1	45	0
Highly Accelerated Temperature and Humidity Stress Test (HAST) [1]	JESD22-A110	130C 85%RH 33.3 psia, Biased, 96 Hours	ADUCM430	Q18956.1.HA1	32	0
				Q18956.2.HA2	32	0
				Q18956.3.HA3	32	0
Solder Heat Resistance (SHR) [1]	J-STD-020	MSL-3	ADUCM430	Q18956.1.SH1	11	0
				Q18956.2.SH2	11	0
				Q18956.3.SH3	11	0
Temperature Cycling (TC) [1]	JESD22-A104	-65/150°C, Soak1, 500 Cycles	ADUCM430	Q18956.1.TC1	32	0
				Q18956.2.TC2	32	0
				Q18956.3.TC3	32	0
Unbiased HAST (UHST) [1]	JESD22-A118	130C 85%RH 33.3 psia, 96 Hours	ADUCM430	Q18956.1.UH1	32	0
				Q18956.2.UH2	32	0
				Q18956.3.UH3	32	0

[1] These samples were subjected to preconditioning (per J-STD-020 Level 3) prior to the start of the stress test. Level 3 preconditioning consists of the following: Bake: 24 hrs @ 125°C, Unbiased Soak: 192 hrs @ 30°C, 60%RH, Reflow: 3 passes through an oven with a peak temperature of 260°C.

Table 2: 0.152um at TSMC Fab-10 Fab Qualification Test Results

Test Name	Specification	Conditions	Device	Lot #	Sample Size	Qty. Failures
Early Life Failure Rate (ELFR)	MIL-STD-883, M1015	125°C, 48 Hours	ADPD4200	Q18200.1.EL1a	667	0
				Q18200.2.EL2a	667	0
				Q18200.3.EL3a	667	0
High Temperature Operating Life (HTOL) [1]	JESD22-A108	125°C<Tj<135°C, Biased, 1,000 Hours	ADUCM430	Q17666.1.HO1	77	0
				Q17666.2.HO2	77	0
				Q17666.3.HO3	77	0
High Temperature Operating Life (HTOL)	JESD22-A108	125°C<Tj<135°C, Biased, 1,000 Hours	ADPD4200	Q18200.1.HO1	45	0
				Q18200.2.HO2	45	0
				Q18200.3.HO3	45	0
			ADPD6000	Q18722.1.HO1	45	0
				Q18722.2.HO2	45	0
				Q18722.3.HO3	45	0
High Temperature Storage Life (HTSL)	JESD22-A103	150°C, 1,000 Hours	ADUCM430	Q18956.1.HS1	45	0
			ADPD4200	Q18200.1.HS1	45	0
			ADPD6000	Q18722.1.HS1	45	0
Highly Accelerated Temperature and Humidity Stress Test (HAST) [1]	JESD22-A110	130C 85%RH 33.3 psia, Biased, 96 Hours	ADUCM430	Q18956.1.HA1	32	0
				Q18956.2.HA2	32	0
				Q18956.3.HA3	32	0
Highly Accelerated Temperature and Humidity Stress Test (HAST)	JESD22-A110	130C 85%RH 33.3 psia, Biased, 96 Hours	ADPD4200	Q18200.1.HA1	45	0
				Q18200.2.HA2	45	0
				Q18200.3.HA3	45	0
			ADPD6000	Q18722.1.HA1	45	0
				Q18722.1.HA3	45	0
				Q18722.2.HA2	45	0

[1] These samples were subjected to preconditioning (per J-STD-020 Level 3) prior to the start of the stress test. Level 3 preconditioning consists of the following: Bake: 24 hrs @ 125°C, Unbiased Soak: 192 hrs @ 30°C, 60%RH, Reflow: 3 passes through an oven with a peak temperature of 260°C.

Samples of the many devices manufactured with these package and process technologies are continuously undergoing reliability evaluation as part of the ADI Reliability Monitor Program. Additional qualification data is available on Analog Devices' web site.

ESD Test Results

The results of Human Body Model (HBM) and Field-Induced Charged Device Model (FICDM) ESD testing are summarized in Table 3. ADI measures ESD results using stringent test procedures based on the specifications listed. Any comparison with another supplier's results should ensure that the same ESD test procedures have been used. For further details, please see the EOS/ESD chapter of the ADI Reliability Handbook (available via the 'Quality and Reliability' link on Analog Devices' web site).

Table 3: ADUCM430 ESD Test Results

ESD Model	Package	ESD Test Spec	RC Network	Highest Pass Level	First Fail Level	Class
FICDM	121-CSP_BGA	JS-002	1Ω, Cpkg	±1250V	NA	C3
HBM	121-CSP_BGA	ESDA/JEDEC JS-001-2011	1.5kΩ, 100pF	±2500V	±3000V	2

Latch-Up Test Results

Three samples of the ADUCM430 were latch-up tested at T_A=25°C per JEDEC Standard JESD78, Class I. All pins passed.

Passing Positive Current	Passing Negative Current	Passing Over-Voltage
+200mA	-200mA	3.63, -3.63V

Approvals

Reliability Engineer: Leo Ouano

Additional Information

Data sheets and other additional information are available on Analog Devices' web site